REMARKS

Claims 1-3 and 5-15 are pending in the present application. Claims 1, 3 and 5-15 have been amended. Claims 4, 16 and 17 have been canceled.

Drawings

The drawings have been objected to under 37 C.F.R. 1.83(a) as allegedly failing to show every feature of the invention specified in the claims. The Examiner has required illustration of the metal pad and molding resin as featured in the independent claims. This objection is respectfully traversed for the following reasons.

In prior art Fig. 1 of the present application, metal pad 14 and molding resin 24 are shown. It should be understood that the connecting portions 240, 340, 440 and 540 as respectively illustrated in Figs. 5, 6, 7 and 9 are incorporated into the semiconductor package as illustrated in Figs. 1 and 2. Accordingly, all features of the claims are illustrated in the figures as taken together. Applicant therefore respectfully submits that the drawings are in compliance with 37 C.F.R. 1.83(a), and thus respectfully urges the Examiner to withdraw this objection for at least these reasons.

Responsive to the Examiner's requirement, the drawings have been corrected as indicated in red ink in the attached annotated marked-up drawings, whereby Figs. 1-4 have been denoted as "PRIOR ART". Also, the conductive post in Fig. 3 has been denoted by reference numeral 20, as described in paragraph [0018] of the present application. The above noted drawing corrections have been incorporated into the

formal Replacement Sheets enclosed herewith. **Th Examin r is respectfully requested to acknowledge receipt and approval of the corrected formal drawings.**

Specification

The disclosure has been objected to in view of the informality as stated on page 3 of the current Office Action dated July 9, 2003. The specification has been amended in view of the above noted informality. The Examiner is therefore respectfully requested to withdraw this objection to the disclosure.

Claim Objections

Claims 1, 5, 9 and 12 have been objected to in view of the informalities as stated on page 3 of the current Office Action. The claims have been amended to improve form in view of the Examiner's suggestions. The Examiner is therefore respectfully requested to withdraw the objection to the claims.

Claim Rejections-35 U.S.C. 103

Claims 1-3 and 12-14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Nishimoto reference (U.S. Patent No. 5,289,036) in view of the Takao et al. reference (Japanese Patent Publication No. 2000-183214). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The chip-size semiconductor package of claim 1 includes in combination a conductive wiring pattern "formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern", a conductive post "which is formed in the molding resin and is connected to the conductive wiring pattern", and a connecting portion "between the conductive wiring pattern and the conductive post, the connecting portion having width that gradually decreases toward the conductive wiring pattern, the connecting portion having a slit to disperse stress to be applied to the connecting portion". Applicant respectfully submits that the chip-size semiconductor package of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

In Figs. 1A and 1B of the Nishimoto reference as primarily relied upon by the Examiner, slit SA is formed along substantially the entirety of wiring layer 108A, to split wiring layer 108A along its length into sub-wiring layers 108A-1 and 108A-2. Similarly, slit SB is formed along substantially the entirety of wiring layer 108B, to split wiring layer 108B along its length into sub-wiring layers 108B-1 and 108B-2. In a similar manner, wiring layer 208A in Fig. 3 of the Nishimoto reference includes a plurality of slits S substantially along an entirety of its length, to provide sub-wiring layers 208A-1 through 208A-3. These various slits are provided for the expressed purpose of preventing slide of the wiring layers.

The Nishimoto reference as relied upon by the Examiner does not specifically disclose a connecting portion **between** a conductive wiring pattern and a conductive

post, wherein the connecting portion has width that gradually decreases toward a conductive wiring pattern and wherein the connecting portion has a slit to disperse stress applied to the connecting portion. Particulary, the slits in the Nishimoto reference are provided along the entirety of the wiring layers, not specifically in a connecting portion of gradually decreasing width between a wiring pattern and a conductive post for dispersing stress applied to the connecting portion.

The Examiner has secondarily relied upon the Takao et al. reference in connection with this rejection. However, slits 6A as illustrated in Fig. 2 of the Takao et al. reference are formed along the entirety of wiring layer 6. The Takao et al. reference does not disclose a connecting portion located between a wiring pattern and a conductive post, wherein the connecting portion has width that gradually decreases toward the conductive pattern and includes slits formed therein for dispersing stress applied to the connecting portion. Applicant therefore respectfully submits that the chip-size semiconductor package of claim 1 would not have been obvious in view of the prior art as relied upon by Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 1-3, is improper for at least these reasons.

With regard to dependent claim 3, the prior art as relied upon by the Examiner does not disclose slits formed in a connecting portion, wherein the slits that are rectangular shaped and arranged to extend radially away from each other. Particularly, the various slits as shown in the Nishimoto and Takao et al. references are substantially arranged parallel with respect to each other. The various slits are not arranged

to extend radially away from each other and thus do not disperse stress in a connecting portion of gradually decreasing width as in claim 3. Applicant therefore respectfully submits that the chip-size semiconductor package of claim 3 would not have been obvious in view of the prior art as relied upon by the Examiner for at least these additional reasons.

The chip-size semiconductor package of claim 12 includes in combination a conductive wiring pattern "formed on the wafer coat, in which the metal pad is electrically connected to the conductive wiring pattern", a conductive post "which is formed in the molding resin and is connected to the conductive wiring pattern", and a connecting portion "between the conductive wiring pattern and the conductive post, the connecting portion having a first region extending outwardly from the conductive post and a second region extending in a perpendicular direction from the first region". Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

The Examiner has interpreted wiring layers 108Ba and 108Bb as illustrated in Fig. 1A of the Nishimoto reference as the second regions of claim 12. However, these wiring layers 108Ba and 108Bb merely extend from wiring layer 108B-2 to through-holes C3 and C2 to be respectively connected to substrate 101 and source-drain region 106N. Wiring layers 108Ba and 108Bb in Fig. 1A of the Nishimoto reference do not extend outwardly in a perpendicular direction from a first region of a connecting portion that is formed between a conductive wiring pattern and a conductive post. Wiring

layers 108Ba and 108Bb extend from portions along the major length of wiring layer 108B-2, not from an intermediate connecting portion. The prior art as relied upon by the Examiner thus fails to meet all the features of claim 12. Applicant therefore respectfully submits that the chip-size semiconductor package of claim 12 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 12-14, is improper for at least these reasons.

Claims 5-7 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Nishimoto reference in view of the Takao et al. reference, in further view of the Owada et al. reference (U.S. Patent No. 5,220,199). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The chip-size semiconductor package of claim 5 includes in combination a conductive wiring pattern and a conductive post as noted above, and a connecting portion "between the conductive wiring pattern and the conductive post". The chip-size semiconductor package further includes in combination a dummy pattern "arranged adjacent along sides of the connecting portion". Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

The Examiner has acknowledged that the Nishimoto and Takao et al. references do not include dummy patterns. The Examiner has interpreted aluminum wirings 7a in Figs. 4 and 7 of the Owada et al. reference as dummy patterns, and has alleged that it would have been obvious to modify the previously relied upon prior art in view of the

Owada et al. reference to meet the features of claim 5. However, wiring 7a as illustrated in Fig. 4 of the Owada et al. reference is directly coupled to aluminum wiring 25a, and ultimately in contact with base region 14. Wiring 7a of the Owada et al. reference therefore is not a dummy layer, because wiring layer 71 provides connection within the integrated circuit.

As further described beginning in column 3, line 62 of the Owada et al. reference, the dummy pattern is disposed so that the corresponding area of inter-level insulator film becomes high, so that the entire surface of the inter-level insulator film formed on the upper layer wiring is made flat. This is done so that step or level gradations may be avoided. As specifically described in column 7, lines 3-12 of the Owada et al. reference with respect to Fig. 4, because of dummy patterns 8, the surface of insulator film 29 below solder bump 2 is made substantially flat throughout.

Clearly, wiring 7a and/or dummy patterns 8 of the Owada et al. reference are not arranged **adjacent along** sides of a connecting portion between a conductive wiring pattern and a conductive post, as would be necessary to meet the features of claim 5. Particularly, the dummy patterns are formed below solder ball 2 and aluminum wiring 3. Even if motivation existed for modifying the previously relied upon prior art in view of the Owada et al. reference (which motivation Applicant does not admit exists), the various dummy patterns would be arranged under the corresponding wiring layers, not adjacent along sides of a connecting portion between a conductive wiring pattern and a conductive post. Accordingly, Applicant respectfully submits that the chip-size

semiconductor package of claim 5 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 5-7, is improper for at least these reasons.

Claims 9 and 10 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Nishimoto reference and the Takao et al. reference, in further view of the Bertolet et al. reference (U.S. Patent No. 5,844,317). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The chip-size semiconductor package of claim 9 includes in combination a conductive wiring pattern and a conductive post as noted previously, and a connecting portion "between the conductive wiring pattern and the conductive post". As further featured, a dent is formed at and around the connecting portion. Applicant respectfully submits that the chip-size semiconductor package of claim 9 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

The Examiner has acknowledged that the previously relied upon prior art does not include a dent as featured in claim 9. The Examiner has apparently interpreted aperture 13 in Figs. 1 and 2 of the Bertolet et al. reference as a dent, and has alleged that it would have been obvious to modify the previously relied upon prior art to meet the features of claim 9 in view of the Bertolet et al. reference.

However, as described beginning in column 7, line 60 of the Bertolet et al. reference, aperture 13 illustrated in Figs. 1 and 2 is formed in passivation layer 12 to

expose upper surface 29 of wire bond pad 28. One of ordinary skill would have no motivation to modify the previously relied upon prior art to include an aperture such as in the Bertolet et al. reference so as to be "formed at and around" a connecting portion that is located between a conductive wiring pattern and a conductive post. Particularly, aperture 13 of the Bertolet et al. reference is formed in passivation layer 12 merely to enable connection of conductive strap 16 to bond pad 28. There would be no reason to modify the previously relied upon prior art to include an opening in a passivation layer at a connecting portion located between a conductive wiring pattern and a conductive post as in the Bertolet et al. reference for connection to a bond pad, because the conductive wiring pattern instead of the intermediate connecting portion would be provided for connection to a bond pad external of the conductive post. Accordingly, Applicant respectfully submits that the chip-size semiconductor package of claim 9 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 9 and 10, is improper for at least these reasons.

Applicant further respectfully submits that the prior art as specifically relied upon by the Examiner in the additional rejections do not overcome the deficiencies as described above. Accordingly, Applicant respectfully submits that these corresponding rejections are improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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AJT:dmc

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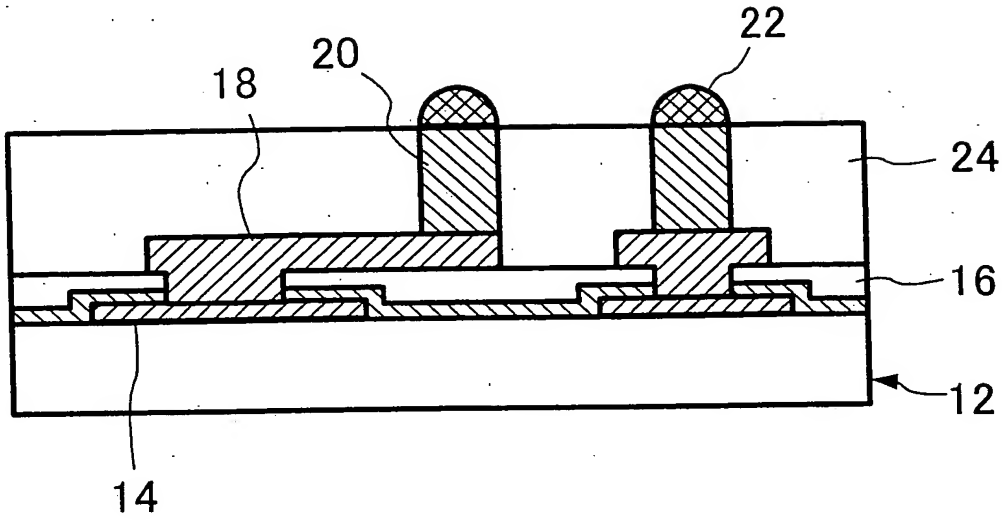
Enclosures: Four (4) sheets of red-inked annotated marked-up drawings
Four (4) replacement sheets

ANNOTATED MARKED-UP DRAWING

Fig. 1

PRIOR ART



ANNOTATED MARKED-UP DRAWING

Fig. 2

PRIOR ART

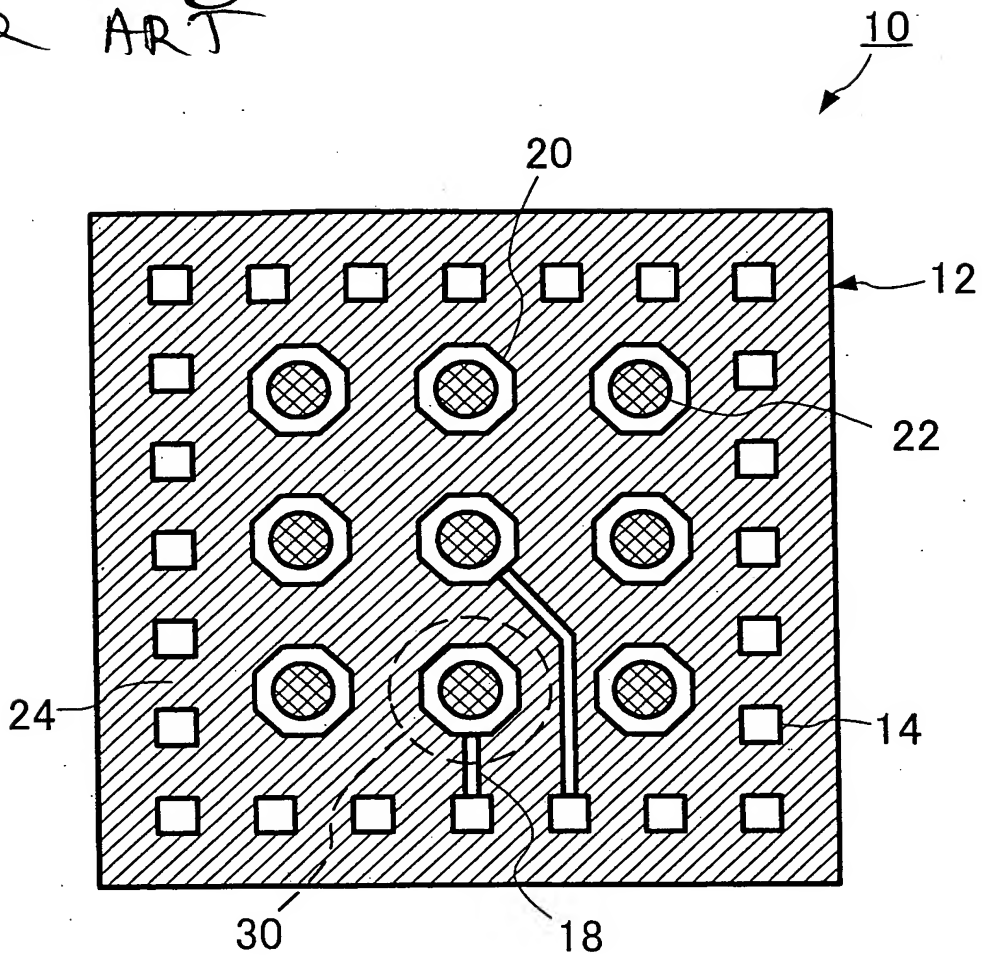
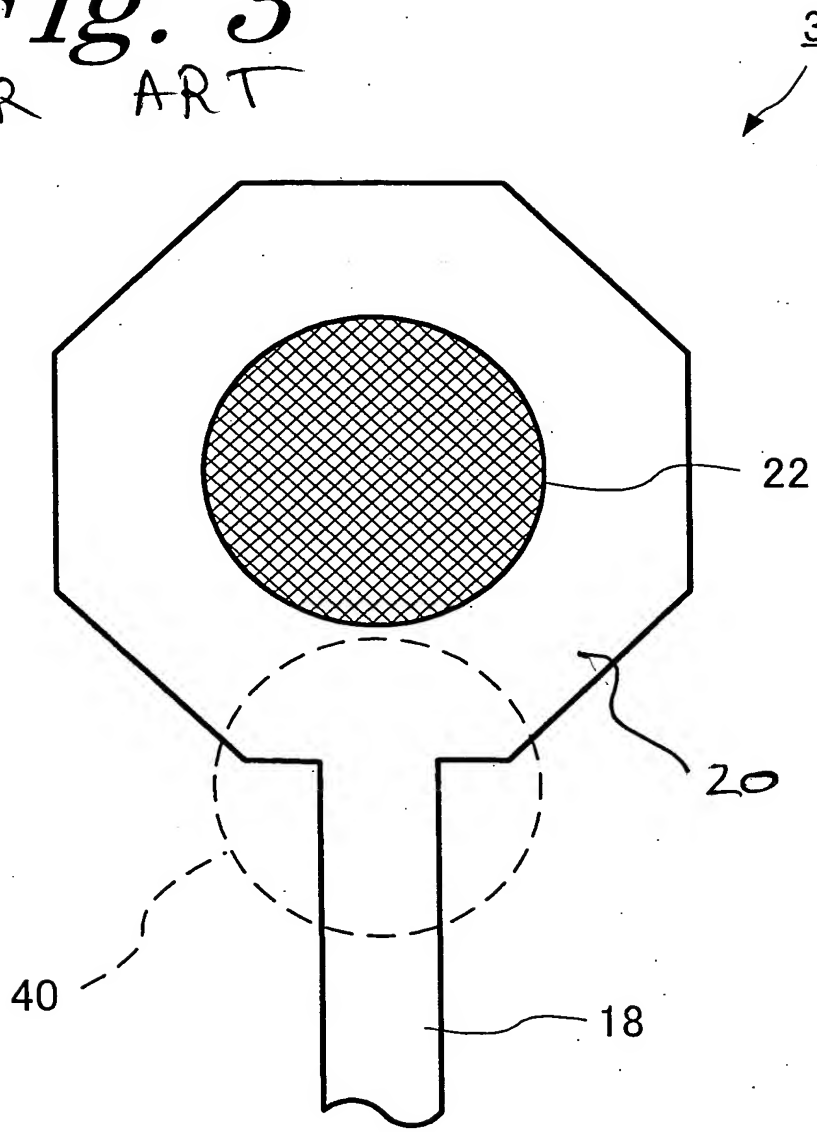


Fig. 3
PRIOR ART



ANNOTATED MARKED-UP DRAWING

Fig. 4

PRIOR ART